AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An electrostatic discharge (ESD) protection circuit for an integrated circuit, the ESD protection circuit comprises:

ESD clamping circuit operably coupled to a first power pin of the integrated circuit and a second power pin of the integrated circuit;

ESD triggering circuit operably coupled to the ESD clamping circuit, wherein, when enabled and when sensing an ESD event, the ESD triggering circuit provides a clamping signal to the ESD clamping circuit such that the ESD clamping circuit provides a low impedance path between the first and second power pins, the ESD triggering circuit having a first time response to sense the ESD event and a second time response for the clamping signal to activate the ESD clamping circuit, in which the first time response is different than the second time response; and

ESD disabling circuit operably coupled to disable the ESD triggering circuit when the integrated circuit is in a normal operating mode.

2. (original) The ESD protection circuit of claim 1, wherein the ESD clamping circuit comprises at least one of: a transistor, a surge suppressor, and a silicon controlled rectifier.

3. (currently amended) The ESD protection circuit of claim 1, wherein the ESD triggering circuit comprises:

an ESD sensing module operably coupled to sense the ESD event and provide a corresponding sensed voltage based on the first time response; and

a timed latch module operably coupled to receive the sensed voltage and provide~~, for a given duration,~~ the clamping signal for a given duration based on the ~~corresponding sensed voltage~~ second time response.

4. (currently amended) The ESD protection circuit of claim 3, wherein the ESD sensing module comprises:

a capacitor having a first node and a second node, wherein the first node of the capacitor is operably coupled to a pin of the integrated circuit that is susceptible to the ESD event; and

a resistor having a first node and a second node, wherein the second node of the resistor is coupled to the first or second power pin of the integrated circuit and the first node of the resistor is coupled to the second node of the capacitor to provide the corresponding sensed voltage, and wherein a time constant of the resistor and the capacitor determines the first time response and is greater than a rise time of the ESD event, is less than a rise time of a power supply of the integrated circuit, and is independent of the given duration of the second time response provided by the time latched module.

5. (original) The ESD protection circuit of claim 3, wherein the timed latch module comprises:

a first NAND gate having a first input, a second input, and an output, the first input of the first NAND gate is coupled to receive the corresponding sensed voltage;

an inverter operably coupled to invert the corresponding sensed voltage to produce an inverted corresponding sensed voltage;

a second NAND gate having a first input, a second input, and an output, wherein the output of the second NAND gate provides the clamping signal and is operably coupled to the second input of the first NAND gate; and

a duration controlled delay module operably coupled to produce a pulse representation of the output of the first NAND gate, wherein the first input of the second NAND gate is operably coupled to receive the pulse representation of the output of the first NAND gate and the second input of the second NAND gate is operably coupled to receive the inverted corresponding sensed voltage.

6. (original) The ESD protection circuit of claim 1 further comprises:

the ESD triggering circuit being operably coupled to an input pin or an output pin of the integrated circuit;

a first diode coupled from the input pin or the output pin to the first power pin; and

a second diode coupled from the input pin or the output pin to the second power pin.

7. (original) The ESD protection circuit of claim 1 further comprises:

a plurality of diode pairs operably coupled to a plurality of input pins and output pins, wherein the ESD triggering circuit is operably coupled to the plurality of diode pairs.

8. (original) The ESD protection circuit of claim 1, wherein the ESD disabling circuit comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the source of the N-channel transistor is coupled to ground of the integrated circuit, wherein the drain of the N-channel transistor is coupled to disable the ESD protection circuit when the N-channel transistor is on; and

delay module operably coupled to enable the N-channel transistor after a delayed sensing of an ESD disable signal.

9. (currently amended) An integrated circuit of use in a multiple function handheld device, wherein the integrated circuit comprises:

a processing module operably coupled to perform at least one algorithm relating to a function of the multiple function handheld device;

a multimedia module operably coupled to produce rendered output data from data corresponding to the processing of the at least one algorithm by the processing module;

at least one input pin operably coupled to the processing module;

at least one output pin operably coupled to the multimedia module; and

electrostatic discharge (ESD) protection circuitry coupled to at least one of the input pin and the output pin, wherein the ESD protection circuitry includes:

ESD clamping circuit operably coupled to a first power pin of the integrated circuit and a second power pin of the integrated circuit;

ESD triggering circuit operably coupled to the ESD clamping circuit, wherein, when enabled and when sensing an ESD event, the ESD triggering circuit provides a clamping signal to the ESD clamping circuit such that the ESD clamping circuit provides a low impedance path between the first and second power pins, the ESD triggering circuit having a first time response to sense the ESD event and a second time response for the clamping signal to activate the ESD clamping circuit, in which the first time response is different than the second time response; and

ESD disabling circuit operably coupled to disable the ESD triggering circuit when the integrated circuit is in a normal operating mode.

10. (original) The integrated circuit of claim 9, wherein the ESD clamping circuit comprises at least one of: a transistor, a surge suppressor, and a silicon controlled rectifier.

11. (currently amended) The integrated circuit of claim 9, wherein the ESD triggering circuit comprises:

an ESD sensing module operably coupled to sense the ESD event and provide a corresponding sensed voltage based on the first time response; and

a timed latch module operably coupled to receive the sensed voltage and provide~~, for a given duration,~~ the clamping signal for a given duration based on the ~~corresponding sensed voltage~~ second time response.

12. (currently amended) The integrated circuit of claim 11, wherein the ESD sensing module comprises:

a capacitor having a first node and a second node, wherein the first node of the capacitor is operably coupled to a pin of the integrated circuit that is susceptible to the ESD event; and

a resistor having a first node and a second node, wherein the second node of the resistor is coupled to the first or second power pin of the integrated circuit and the first node of the resistor is coupled to the second node of the capacitor to provide the corresponding sensed voltage, and wherein a time constant of the resistor and the capacitor determines the first time response and is greater than a rise time of the ESD event, is less than a rise

time of a power supply of the integrated circuit, and is independent of the given duration of the second time response provided by the time latched module.

13. (original) The integrated circuit of claim 11, wherein the timed latch module comprises:

a first NAND gate having a first input, a second input, and an output, the first input of the first NAND gate is coupled to receive the corresponding sensed voltage;

an inverter operably coupled to invert the corresponding sensed voltage to produce an inverted corresponding sensed voltage;

a second NAND gate having a first input, a second input, and an output, wherein the output of the second NAND gate provides the clamping signal and is operably coupled to the second input of the first NAND gate; and

a duration controlled delay module operably coupled to produce a pulse representation of the output of the first NAND gate, wherein the first input of the second NAND gate is operably coupled to receive the pulse representation of the output of the first NAND gate and the second input of the second NAND gate is operably coupled to receive the inverted corresponding sensed voltage.

14. (original) The integrated circuit of claim 9 further comprises:

the ESD triggering circuit being operably coupled to an input pin or an output pin of the integrated circuit;

a first diode coupled from the input pin or the output pin to the first power pin; and

a second diode coupled from the input pin or the output pin to the second power pin.

15. (original) The integrated circuit of claim 9 further comprises:

a plurality of diode pairs operably coupled to a plurality of input pins and output pins, wherein the ESD triggering circuit is operably coupled to the plurality of diode pairs.

16. (original) The integrated circuit of claim 9, wherein the ESD disabling circuit comprises:

an N-channel transistor having a gate, a drain, and a source, wherein the source of the N-channel transistor is coupled to ground of the integrated circuit, wherein the drain of the N-channel transistor is coupled to disable the ESD protection circuit when the N-channel transistor is on; and

delay module operably coupled to enable the N-channel transistor after a delayed sensing of an ESD disable signal.